Order this document
by EB366/D
REV 1

MOTOROLA
digital dna™

Semiconductor Products Sector
Engineering Bulletin

EB366

In-Circuit Programming of FLASH Memory Using the Monitor Mode for the MC68HC908GP32

By Timothy J. Airaudi
Applications Engineering, Microcontroller Division
Austin, Texas

Introduction

This engineering bulletin describes how to perform in-circuit programming (ICP) of the FLASH memory using monitor mode for the MC68HC908GP32.

Two ICP methods are discussed here:

- Using the M68ICS08GP in-circuit simulator (ICS) with P&E Microsystems software
- Using P&E Microsystems software with an external communications circuit

ICP is a process where user code is programmed into the device's FLASH memory after the part has been assembled into the application. ICP also allows the original users code to be erased and re-programmed. This method can be used in development, production/manufacturing, and in a field environment.

intelligence everywhere™

Using Monitor Mode for FLASH Programming

Motorola's current solution for ICP is the in-circuit simulators and P&E's software.

The software and ICS allow programming of the parts on the simulator or in the target circuit via a MON08 ribbon cable. The software also allows programming of the part, without the ICS, by using an external communications circuit.

All the programming described here is accomplished by placing the part into monitor mode. In this mode, erasing and programming are done through a single-wire interface with the host computer.

The two ways to enter monitor mode are:

- The ICS provides the entry requirements into standard monitor mode. These entry requirements must be implemented on the target board if the ICS is not used.
- A second way to enter monitor mode, that does not require a high voltage on the $\overline{\text{IRQ}}$ pin, is forced monitor mode. This mode does not need to meet all the monitor mode entry conditions of the standard monitor mode, but it does require the part to be blank (erased).

This engineering bulletin describes how to connect the part, communicate at different baud rates, place the part into monitor mode, pass security, and erase and program the part. If the security code is not known, the contents of the FLASH can't be read, but the FLASH can be erased and reprogrammed.

Information on the M68ICS08GP can be found at:
http://www.motorola.com/mcu/
P&E Microsystems software can be downloaded free from that company's Web site.

NOTE: *All of the oscillators used in this engineering bulletin are the 4-pin "powered" or "canned" type oscillators. Discussing all the different vendors of crystals, ceramic oscillators, other required external components, and component layout variables would be too extensive.*

ICP Using M68ICS08GP's MON08 Interface

Use this procedure for performing ICP using the ICS's MON08 cable to the target application.

1. Materials required:
   a. PC with P&E's software installed (version 1.32 or higher)
   b. M68ICS08GP simulator
   c. Adapter/connector to connect the female end of the MON08 cable to the target application
   d. Pin assignment diagram (see **Figure 1**, **Figure 2**, and **Figure 3**)
   e. Monitor mode entry requirements (see **Table 1**)
   f. Crystal oscillator on the target or from an external clock source with a value from **Table 2**
   g. Target board must have the ability to perform a power-on reset (POR) not just a reset (required to enter monitor mode).
2. Connections (see **Figure 4**):
   a. 9-pin serial cable from PC to the ICS
   b. 5 volts to the ICS
   c. MON08 cable (even pins) from J6 of the ICS to the target board with these connections:
      — MON08 GND to the V_{SS} pin on the part
      — MON08 RST to the $\overline{RST}$ pin on the part
      — MON08 IRQ to the $\overline{IRQ}$ pin on the part
      — MON08 PTA0 to the PTA0 pin on the part
      — MON08 PTA7 to the PTA7 pin on the part
      — MON08 PTC0 to the PTC0 pin on the part
      — MON08 PTC1 to the PTC1 pin on the part
      — MON08 PTC3 to the PTC3 pin on the part
   d. It is assumed that all V_{DD} and V_{SS} pins on the part are already connected.

3. Operation — Standard monitor mode entry:
   a. Launch P&E's WINIDE in the ICS08GPZ software.
   b. Open desired file. (Demo file can be used for testing purposes.)
   c. Assemble/Compile the file (see **Figure 8**).
   d. Plug in power to the ICS.
   e. Turn on power to the target.
   f. Launch the programmer.
   g. From "Target Hardware Type," select "Class II" (see **Figure 9**).
   h. From "PC Serial Port Configuration," select the PC port you are using and the appropriate baud rate (see **Table 2**).
   i. From "Target MCU Security Bytes," select appropriate security code (blank part = FF).
   j. Select "Contact Target with these Settings…"
   k. Follow the instructions in the "Power Down/Up Dialog" windows.
   l. Select appropriate algorithm for the part. The high-speed algorithm will not work at 28,800 baud.
   m. Double click on "Erase Module" – EM (see **Figure 10**).
   n. Double click on "Program Module" – PM.
   o. Record security bytes. This information can be seen by quitting and then re-entering the programmer. The S19 record will have the same security bytes as the part just programmed as long as it is not changed. The security bytes consist of the information stored in the interrupt vectors, $FFF6–$FFFD.
4. Operation — Forced monitor mode entry:
   a. Forced monitor mode is not supported by this ICS. However, this mode can be entered by using the procedure found in **ICP Using the External Communications Circuit (No ICS)**.

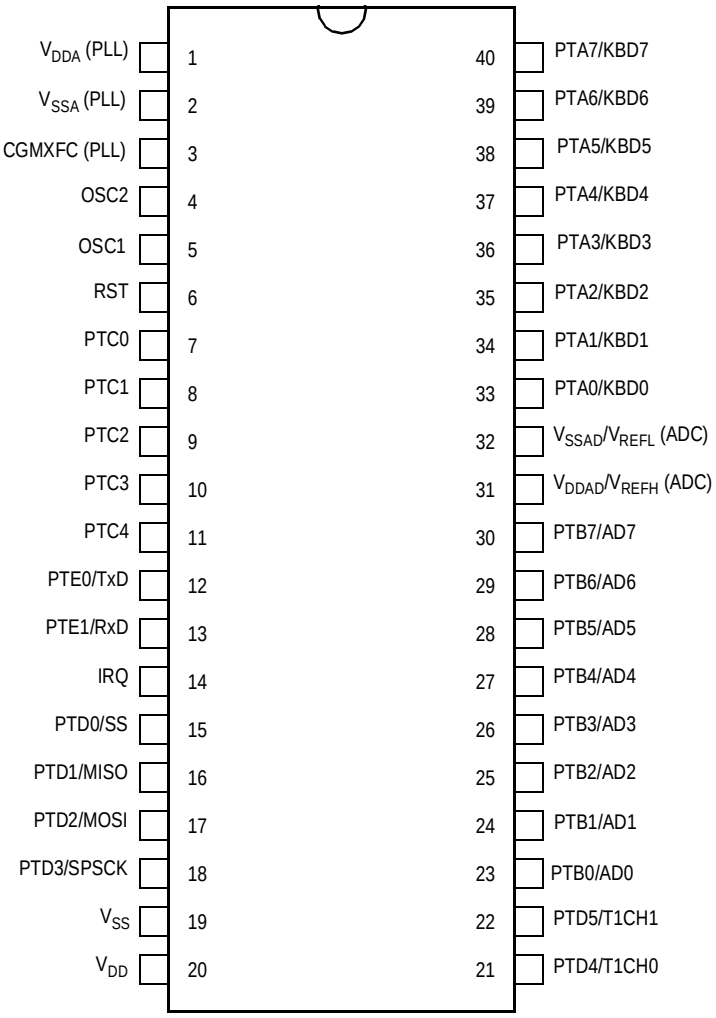
ICP Using the External Communications Circuit (No ICS)

Use this procedure for performing ICP via an external communications circuit in place of this ICS to the target application.

1. Materials required:
   a. PC with P&E software installed (version 1.32 or higher)
   b. Adapter/connector to connect the male end of the 9 pin serial cable to the target application
   c. The external communications circuit. Also needed is a 5-volt power source to power this circuit (see **Figure 5**, **Figure 6**, and **Figure 7**).
   d. Pin assignment diagram (see **Figure 1**, **Figure 2**, and **Figure 3**)
   e. Monitor mode entry requirements (see **Table 1**)
   f. Crystal oscillator on the target or from an external clock source, with a value from **Table 2**
   g. Target board must have the ability to perform a POR not just a reset of the part (required to enter monitor mode).
2. Connections (see **Figure 5**):
   a. 9-pin serial cable from PC to the external communications circuit
   b. V+ pin of the RS-232 part to the $\overline{\text{IRQ}}$ pin of the part
   c. Communication pin of HC125 to PTA0 of the part
   d. Target pin requirements:
      — PTA7 of the part to V_{SS}
      — PTC0 of the part to V_{DD} via a pullup resistor
      — PTC1 of the part to V_{SS}
      — PTC3 of the part to V_{SS} (crystal frequency ÷ 2) or V_{DD} via pullup resistor (crystal frequency ÷ 4). See **Table 2**.
      — $\overline{\text{RESET}}$ has an internal pullup resistor.
   e. It is assumed that all V_{DD} and V_{SS} pins on the part are already connected.

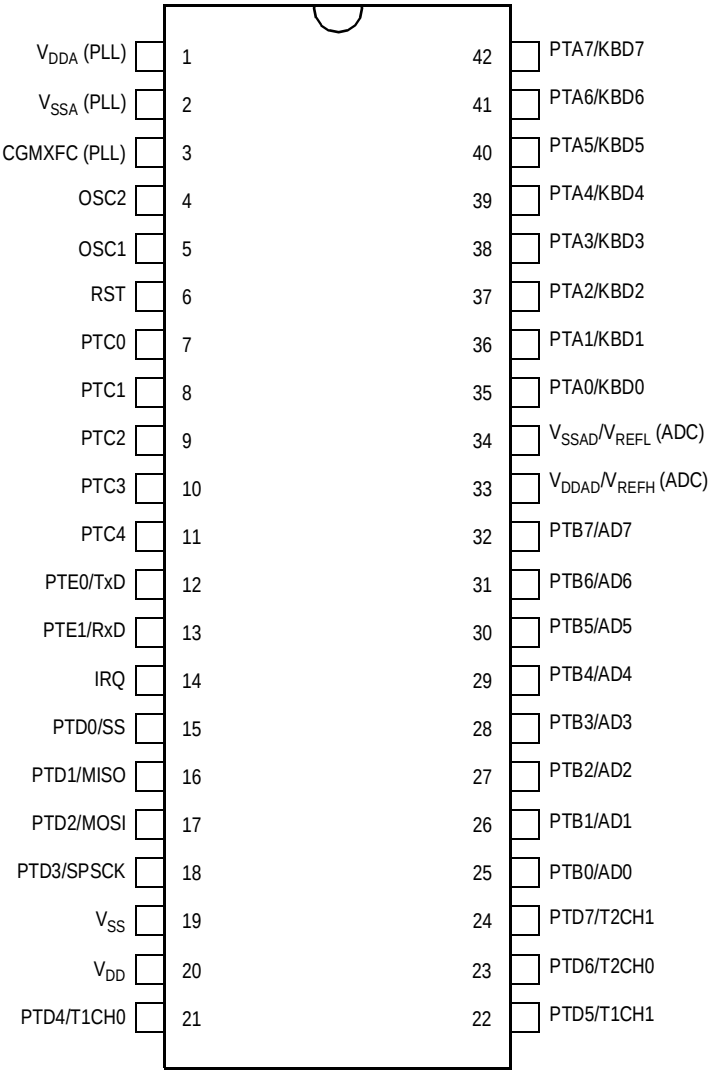
3. Operation — Standard monitor mode entry:
   a. Launch P&E's WINIDE in the ICS08GPZ software.
   b. Open desired file. (Demo file can be used for testing purposes.)
   c. Assemble/Compile the file (see **Figure 8**).
   d. Apply power to the external communications circuit.
   e. Turn on power to the target.
   f. Launch the programmer.
   g. From "Target Hardware Type," select "Class III" (see **Figure 9**).
   h. From "PC Serial Port Configuration," select the PC port in use and the appropriate baud rate (**Table 2**).
   i. From "Target MCU Security Bytes," select appropriate security code (blank part = FF).
   j. Select "Contact Target with these Settings…"
   k. Follow the instructions in the "Power Cycle Dialog" window.
   l. Select appropriate algorithm for the part. The high-speed algorithm will not work at 28,800 baud.
   m. Double click on "Erase Module" – EM (see **Figure 10**).
   n. Double click on "Program Module" – PM.
   o. Record security bytes. This information can be seen by quitting and then re-entering the programmer. The S19 record will have the same security bytes as the part just programmed as long as it is not changed. The security bytes consist of the information stored in the interrupt vectors, $FFF6–$FFFD.

4. Operation — Forced monitor mode entry:
   a. Blank part with oscillator value from **Table 2**. See **Figure 6**.
      — Remove connection to the $\overline{\text{IRQ}}$ pin from V+ of the external communications circuit.
      — No connections to PTC0, PTC1, and PTC3 are necessary in this mode.
      — $\overline{\text{IRQ}}$ has an internal pullup resistor.
      — If the crystal oscillator in the target is not a value listed in **Table 2**, it is possible to "overdrive" the target crystal, with an external clock, for the short duration of the programming sequence. An example would be overdriving a target's 32.768-kHz crystal with a 9.8304-MHz external clock.
   b. Blank part with a 32.768-kHz oscillator. See **Figure 7**.
      — Connect the $\overline{\text{IRQ}}$ pin to V_{SS}.



NOTE: PTC5, PTC6, PTD6, and PTD7 were removed for this package.

Figure 1. 40-Pin PDIP Pin Assignments



NOTE: PTC5 and PTC6 were removed for this package.

Figure 2. 42-Pin SDIP Pin Assignments

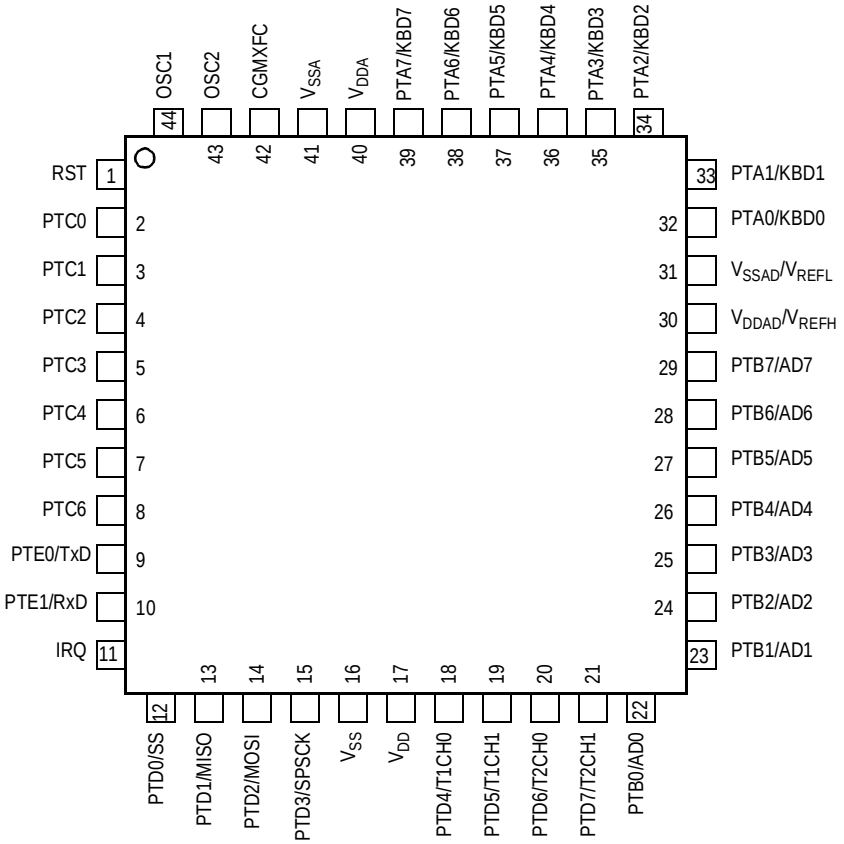


Figure 3. 44-Pin QFP Pin Assignments

Table 1. Monitor Mode Signal Requirements and Options

$\overline{IRQ}$	RESET	$FFFE/ $FFFF	PLL	PTC0	PTC1	PTC3	External Clock(1)	CGMOUT	Bus Frequency	COP	For Serial Communication			Comment
											PTA0	PTA7	Baud Rate(2) (3)	
X	GND	X	X	X	X	X	X	0	0	Disabled	X	X	0	No operation until reset goes high
V_{TST}	V_{DD} or V_{TST}	X	OFF	1	0	0	4.9152 MHz	4.9152 MHz	2.4576 MHz	Disabled	1	0	9600	PTC0 and PTC voltages only required if $\overline{IRQ}$ = V_{TST}; PTC3 determines frequency divider
											X	1	DNA	
V_{TST}	V_{DD} or V_{TST}	X	OFF	1	0	1	9.8304 MHz	4.9152 MHz	2.4576 MHz	Disabled	1	0	9600	PTC0 and PTC1 voltages only required if $\overline{IRQ}$ = V_{TST}; PTC3 determines frequency divider
											X	1	DNA	
V_{DD}	V_{DD}	$FF (blank)	OFF	X	X	X	9.8304 MHz	4.9152 MHz	2.4576 MHz	Disabled	1	0	9600	External frequency always divided by 4
											X	1	DNA	
GND	V_{DD}	$FF (blank)	ON	X	X	X	32.768 kHz	4.9152 MHz	2.4576 MHz	Disabled	1	0	9600	PLL enabled (BCS set) in monitor code
											X	1	DNA	
V_{DD} or GND	V_{TST}	$FF (blank)	OFF	X	X	X	X	—	—	Enabled	X	X	—	Enters user mode — will encounter an illegal address reset
V_{DD} or GND	V_{DD} or V_{TST}	Not $FF (programmed)	OFF	X	X	X	X	—	—	Enabled	X	X	—	Enters user mode

1. External clock is derived by a 32.768-kHz crystal or a 4.9152/9.8304-MHz off-chip oscillator.
2. PTA0 = 1 if serial communication; PTA0 = X if parallel communication
3. PTA7 = 0 Æ serial, PTA7 = 1 Æ parallel communication for security code entry
4. DNA = does not apply, X = don't care

Table 2. Crystal Frequency vs Baud Rate

Divide by 2 Option (PTC3 to Development Tool or V_{SS})		
Crystal Frequency (MHz)	**Internal Bus Frequency (MHz)**	**Baud Rate**
2.4576	1.2288	4800
4.9152	2.4576	9600
7.3728	3.6864	14,400
9.8304	4.9152	19,200
14.7456	7.3728	28,800
Divide by 4 Option (PTC3 to V_{DD})		
4.9152	1.2288	4800
9.8304	2.4576	9600
14.7456	3.6864	14,400
19.6608	4.9152	19,200
29.4912	7.3728	28,800

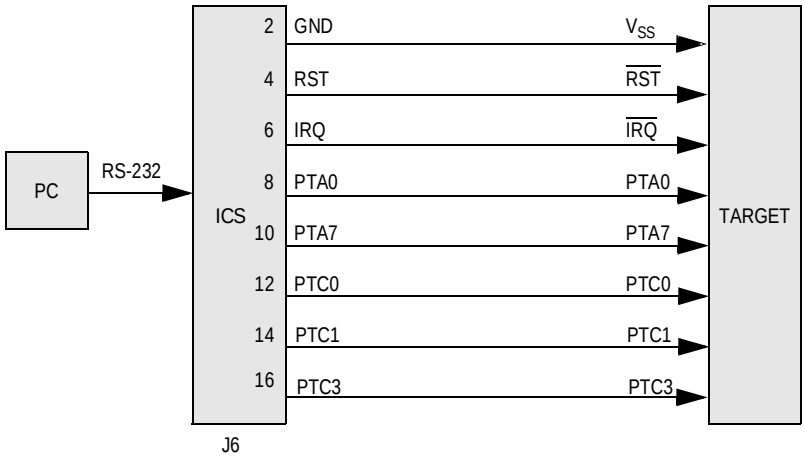


Figure 4. MC68HC908GP32 MON08 Connections

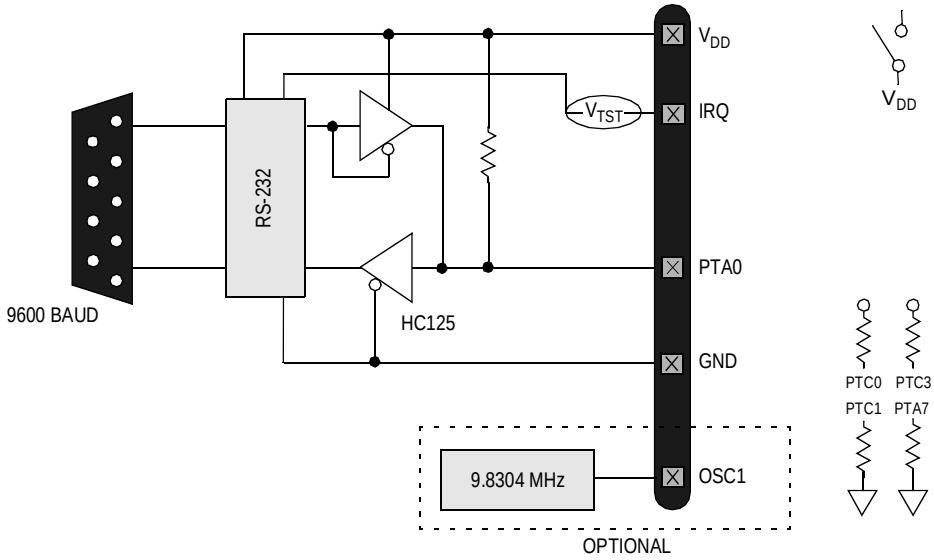


Figure 5. MC68HC908GP32 Standard Monitor Mode (9.8304 MHz)

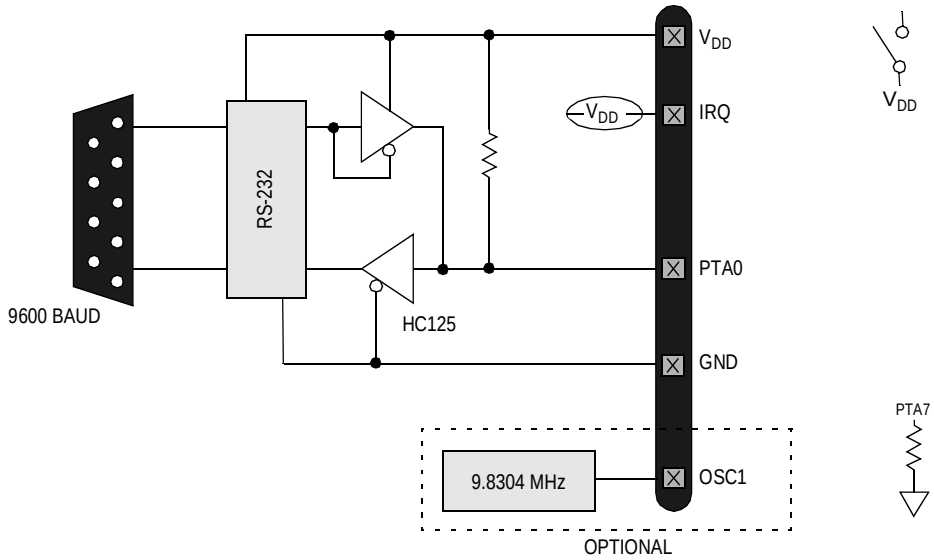


Figure 6. MC68HC908GP32 Forced Monitor Mode (9.8304 MHz)

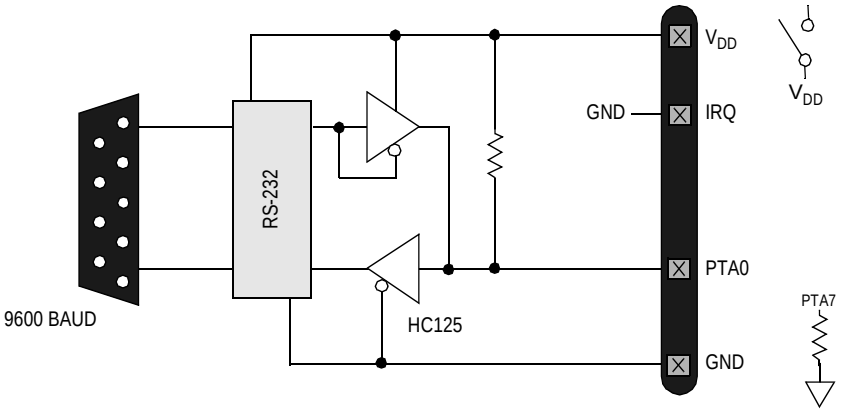
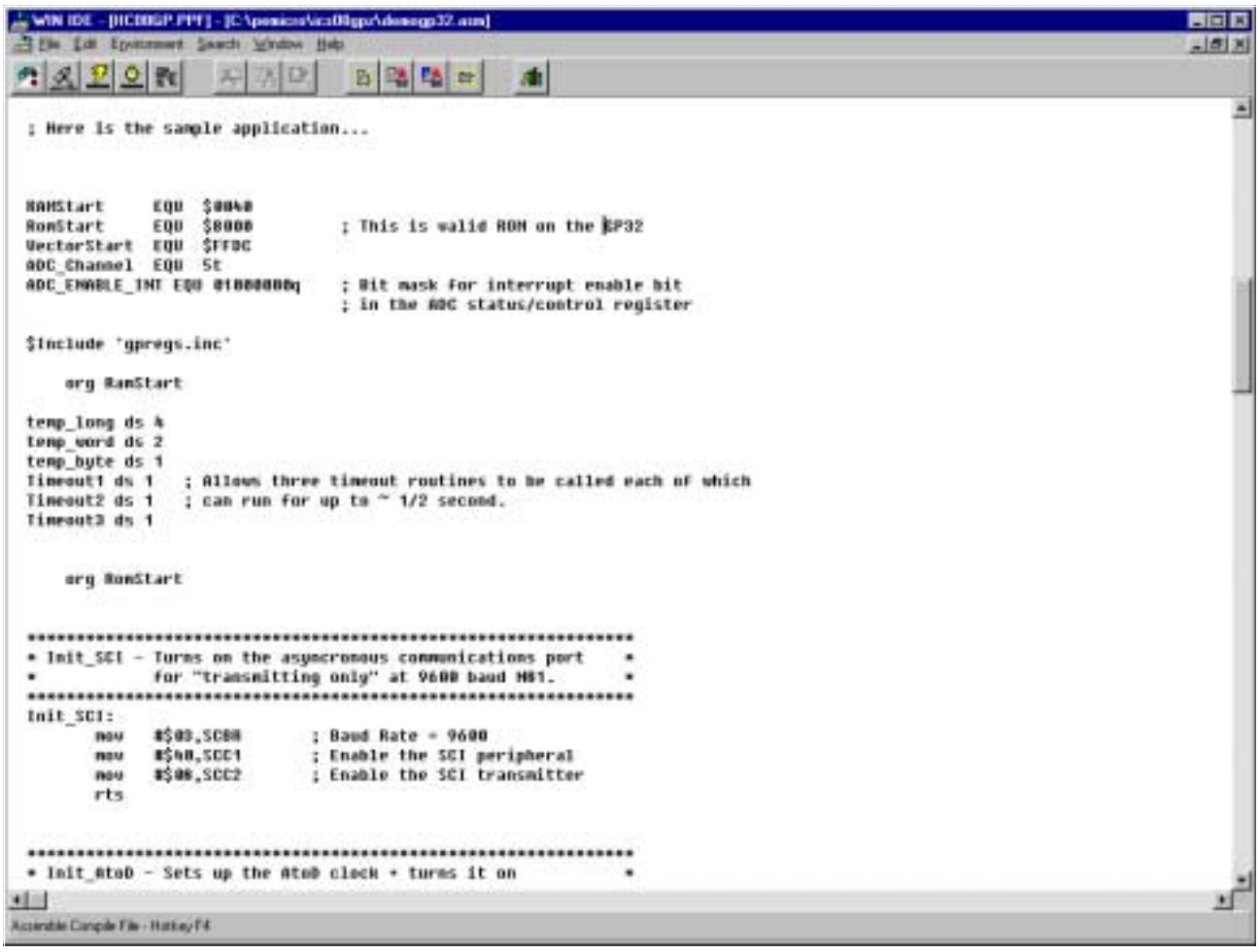


Figure 7. MC68HC908GP32 Forced Monitor Mode (32.768 kHz)



```
; Here is the sample application...


RAMStart     EQU  $0040
RomStart     EQU  $8000         ; This is valid ROM on the GP32
VectorStart  EQU  $FFDC
ADC_Channel  EQU  5t
ADC_ENABLE_INT EQU @10000000b    ; Bit mask for interrupt enable bit
                                 ; in the ADC status/control register

$Include 'gpregs.inc'

    org RamStart

temp_long ds 4
temp_word ds 2
temp_byte ds 1
Timeout1 ds 1   ; Allows three timeout routines to be called each of which
Timeout2 ds 1   ; can run for up to ~ 1/2 second.
Timeout3 ds 1


    org RomStart


*************************************************************
* Init_SCI - Turns on the asyncronous communications port    *
*          for "transmitting only" at 9600 baud MBI.         *
*************************************************************
Init_SCI:
       mov   #$03,SCBR       ; Baud Rate = 9600
       mov   #$40,SCC1       ; Enable the SCI peripheral
       mov   #$08,SCC2       ; Enable the SCI transmitter
       rts


*************************************************************
* Init_AtoD - Sets up the AtoD clock + turns it on          *
```

Figure 8. P&E's WINIDE Window

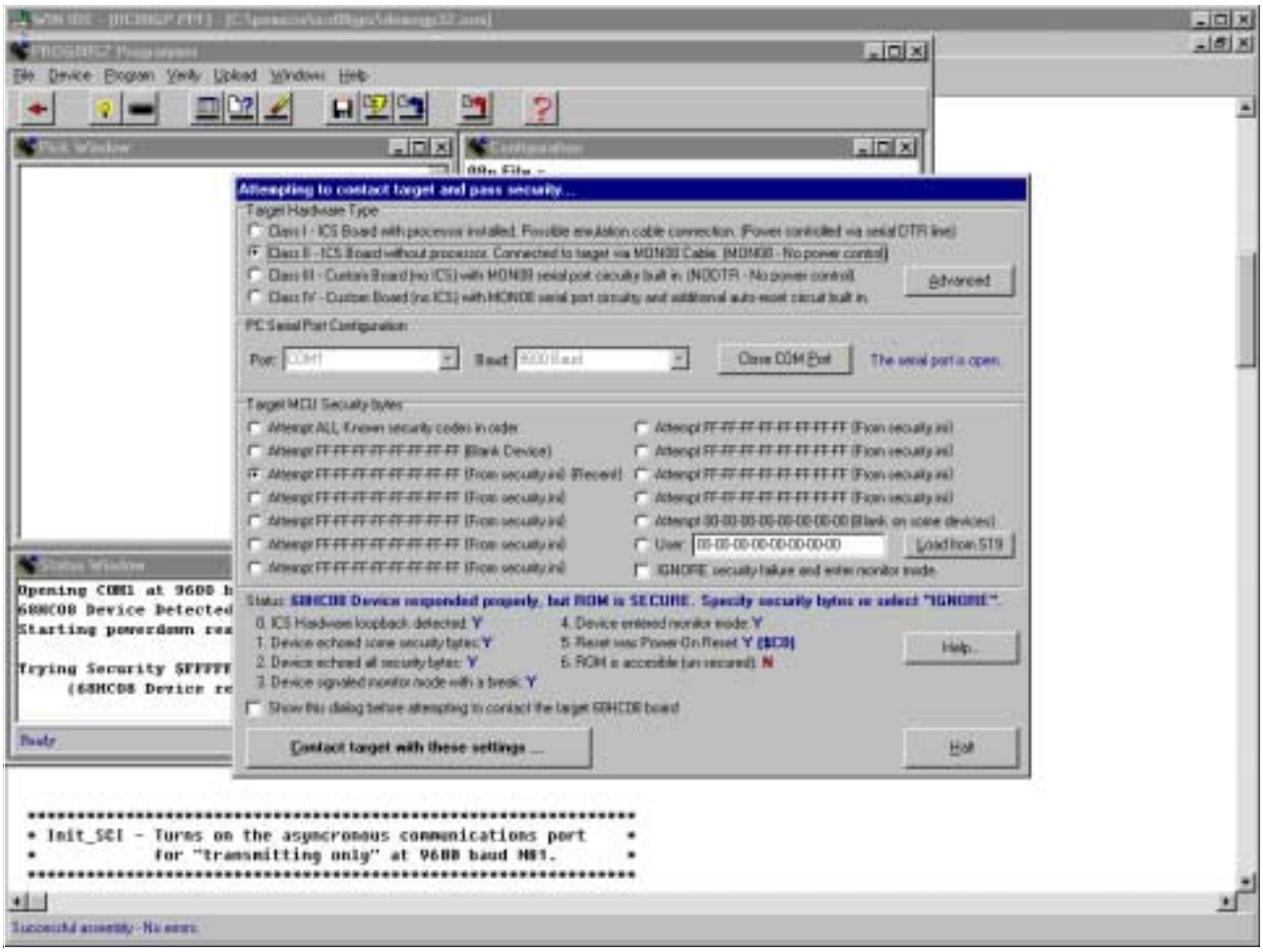


Figure 9. P&E's Target and Security Window

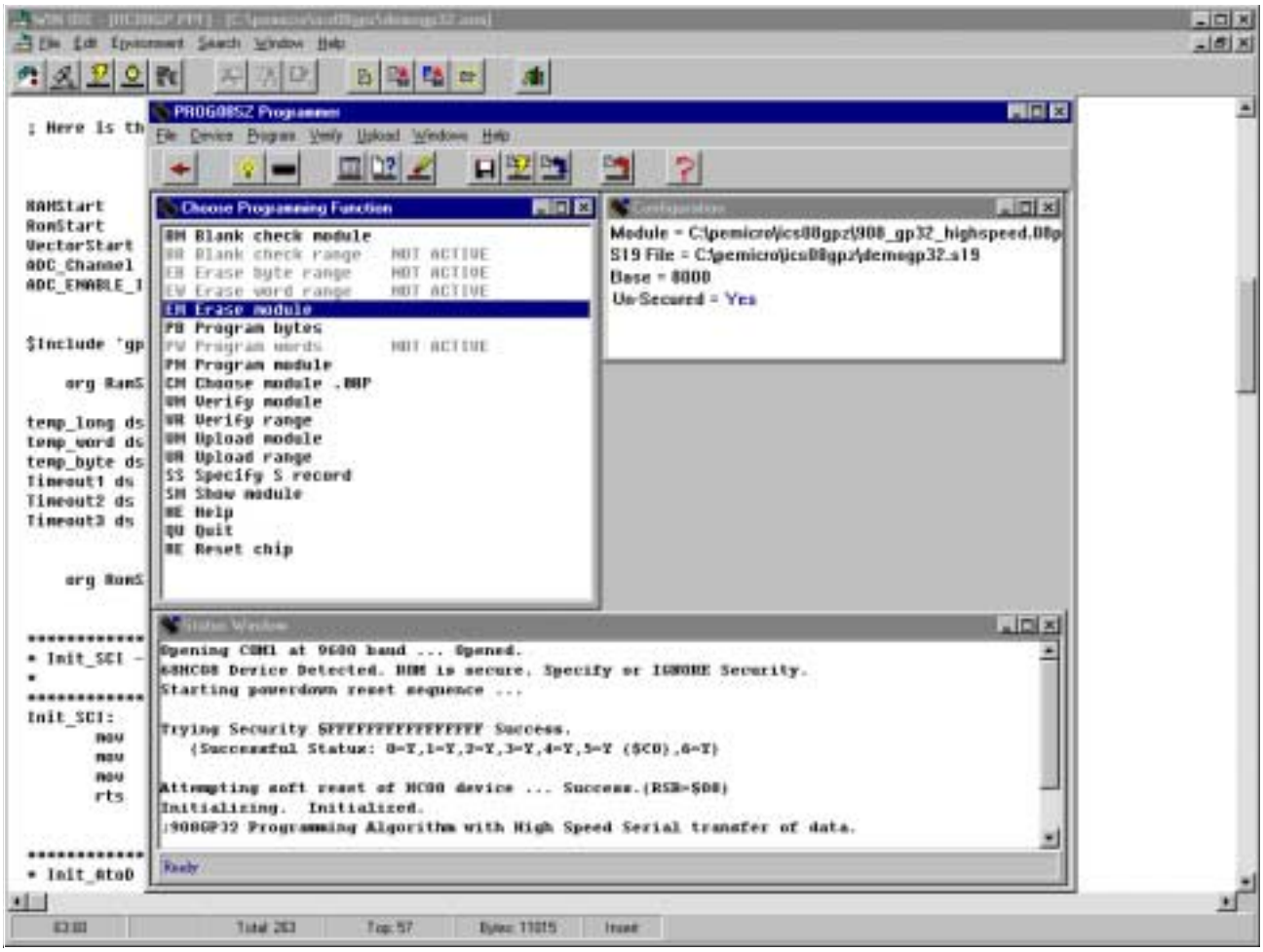


Figure 10. P&E's Programmer Window

How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 5405, Denver, Colorado 80217. 1-303-675-2140 or 1-800-441-2447

JAPAN: Motorola Japan Ltd.; SPS, Technical Information Center, 3-20-1, Minami-Azabu, Minato-ku, Tokyo 106-8573 Japan. 81-3-3440-3569

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong. 852-26668334

Technical Information Center: 1-800-521-6274

HOME PAGE: http://www.motorola.com/semiconductors/