Tutorial Introduction

PURPOSE

- To explain how to configure and use the Low Voltage Inhibit Module

OBJECTIVES:

- Describe the uses and features of the Low Voltage Inhibit Module.
- Identify the steps to configure the Low Voltage Inhibit Module.

CONTENTS:

- 7 pages
- 1 question

LEARNING TIME:

- 10 minutes

PREREQUISITE:

- Training modules: 68HC08 CPU, Resets and Interrupts

Welcome to this tutorial on the 68HC08 Low Voltage Inhibit (LVI) Module. This tutorial describes the features and configuration of the LVI Module. Please note that on subsequent pages, you will find reference buttons in the upper right of the content frame that access additional content.

Upon completion of this tutorial, you'll be able to describe the uses and features of the LVI Module. You'll also be able to configure the LVI Module to protect the MCU system during a power voltage drop.

The recommended prerequisites for this tutorial are the 68HC08 CPU and the Resets and Interrupts training modules. Click the Forward arrow when you're ready to begin the tutorial.

LVI Module Uses and Features

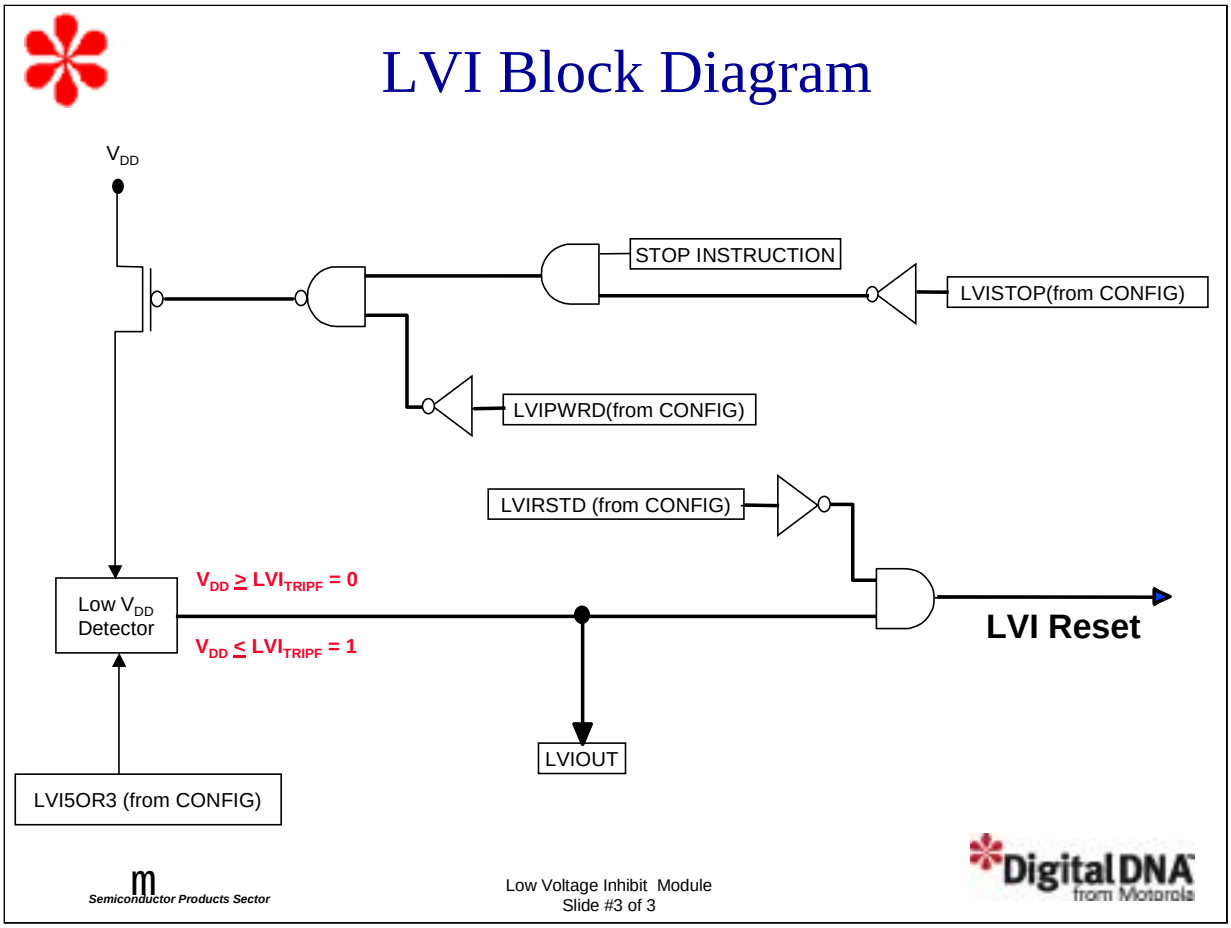
- Improves system reliability
- Reduces component count and cost
- Resets MCU when the voltage drops
- Resumes MCU operation when voltage rises
- Includes selectable trip voltage for 3V and 5V systems

Let's begin this tutorial with a discussion of the uses and features of the Low Voltage Inhibit (LVI) Module.

Reliable system operation can be affected as the supply voltage drops. A brown-out condition or a supply battery nearing the end of its life are common causes of inconsistent supply voltage. The LVI Module protects MCU system operation during these types of events. Because external LVI circuits typically cost over $0.30, integrating this function on-chip reduces system cost.

When the LVI circuit detects the falling voltage, it can reset the CPU thereby avoiding erratic CPU behavior. As proper voltage returns to the circuit, the CPU resumes processing. This helps to avoid potential system errors.

Most 68HC08 derivatives allow the user to select one of two LVI trip points to support 5V and 3V systems. For more information about the specific trip points for a particular MCU derivative, see the electrical specifications section of the MCU technical data book.



Next, let's look at how to configure the LVI Module.

The LVI Module contains a bandgap reference circuit and a comparator to determine when the MCU operating voltage drops below the specified trip point values. The LVI Module is enabled out of reset and configured using several bits in the system configuration register (CONFIG). This register is typically initialized at power-on reset. Once written to, the register can't be written to again until the next reset occurs. This write-once feature ensures that an application won't inadvertently reconfigure the MCU.

The LVI power disable bit, LVIPWRD, enables the LVI module to monitor V_{DD} voltage. By clearing this bit, power is applied to the LVI analog circuit. Setting the LVIPWRD bit to 1 will stop current drain from the LVI Module.

The LVI enable in stop mode bit, LVISTOP, determines whether the LVI operates in stop mode. When the LVIPWRD bit is cleared, setting the LVISTOP bit to 1 enables the LVI Module to operate during stop mode. A reset clears the LVISTOP bit. The ability to automatically disable the LVI in STOP mode allows for reduced power consumption and longer battery life while still protecting the CPU during normal operation.

The LVI 5 V or 3 V operating mode bit, LVI5OR3, selects the voltage operating mode of the LVI Module. Note that the LVI voltage mode must match the operating voltage, V_{DD}. Setting the LVI5OR3 bit to 1 configures the trip point voltage (V_{TRIPF}) for 5 V nominal operation. Clearing the LVI5OR3 bit configures V_{TRIPF} for 3 V nominal operation. On reset, the LVI defaults to 3V mode. If running a 5 V system, the LVI5OR3 bit is typically set to raise the trip point for 5V operation after every power-on reset. The trip point values are typically in the 4.2 V to 4.5 V range in 5 V mode or 2.4 V to 2.7 V range in 3 V mode. For information about specific trip point values, see the electrical specifications in the MCU technical data book.

The LVI reset disable bit, LVIRSTD, disables the reset signal from the LVI Module. When the LVIRSTD bit is cleared, the LVI Module will generate a reset when LVIOUT is set, which means V_{DD} has fallen below the falling trip voltage, V_{TRIPF}. If this condition occurs, the MCU will remain in the reset condition until V_{DD} rises above the rising trip voltage, V_{TRIPR}. V_{TRIPF} is lower than V_{TRIPR} by the hysteresis voltage, typically 0.1 V, to avoid entering and exiting reset when the voltage supply has a slight ripple near the trip voltage.

LVI Status Register (LVISR)

Address: $FE0C

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	LVIOUT	0	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

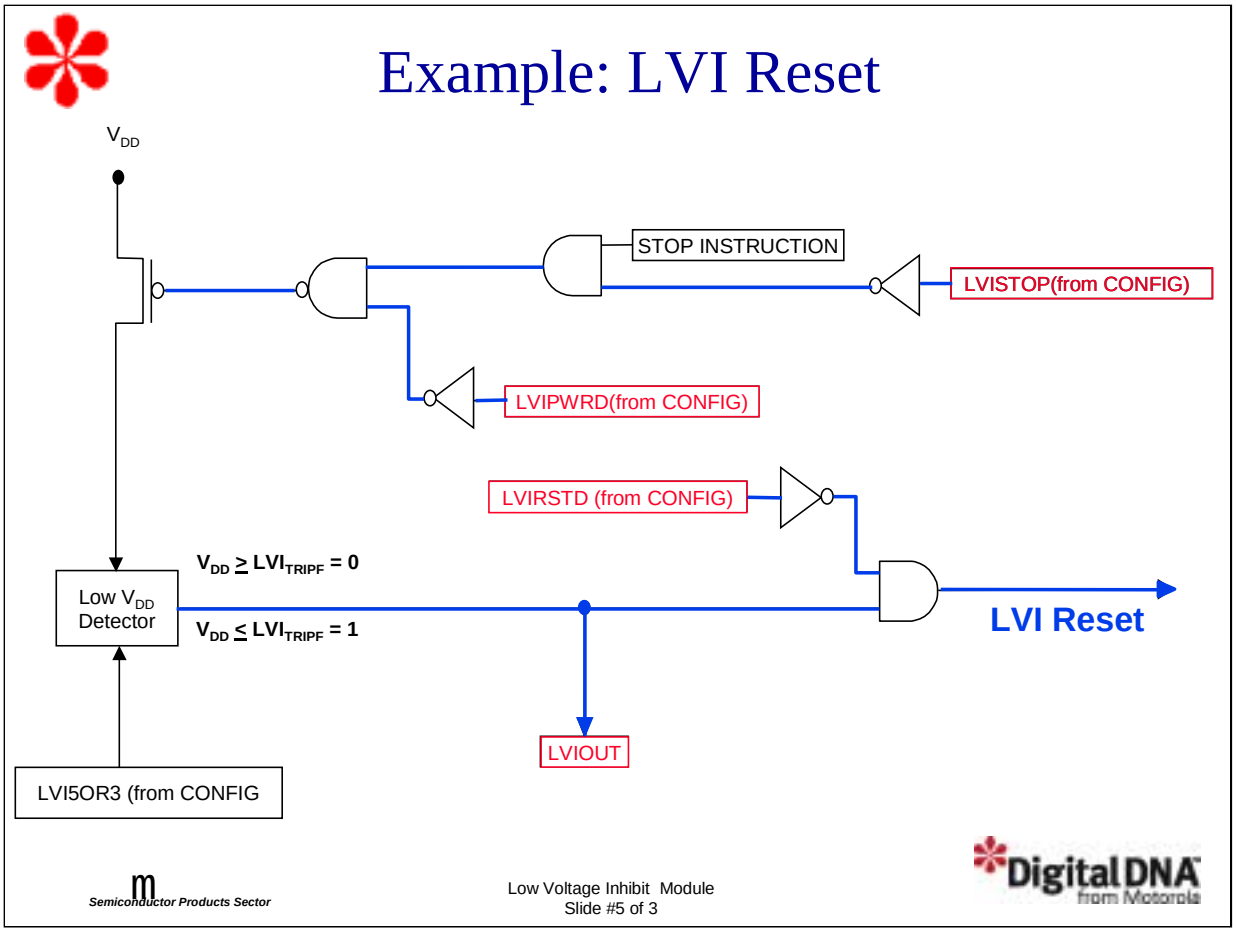
= Unimplemented

LVIOUT — LVI Output Bit
This read-only flag is set when the V_{DD} voltage falls below the V_{TRIPF} trip voltage.

The LVI Module uses the LVI status register (LVISR) to indicate when the V_{DD} voltage falls below the V_{TRIPF} level. The LVI output bit, LVIOUT, is a read-only status flag that the LVI Module sets when V_{DD} is less than V_{TRIPF}. The LVI Module clears the bit when V_{DD} rises above V_{TRIPR}. A reset clears the LVIOUT bit.

This status flag is particularly useful when the LVI Module is used in polled operation mode (not reset driven mode). This mode is normally used in applications where operating V_{DD} levels below the V_{TRIPF} level is desired to extend battery life. In this case, software can monitor V_{DD} by polling the LVIOUT status flag.

To configure the LVI for this mode, enable the LVI Module by setting the LVIPWRD bit to 0 and set the LVIRSTD bit to 1 to disable LVI resets.



Let's look at a simple example.

First, set the LVISTOP bit to 1. This allows the LVI Module to operate during a STOP instruction.

Power is applied to LVI by setting LVIPWRD = 0.

When V_{DD} falls below the trip voltage, V_{TRIPF} , the LVI logic detects this condition and sets the LVIOUT bit to 1.

If LVIRSTD = 0, a reset will be sent to the CPU.

Question

With the LVI Module enabled and the LVIRSTD bit set to 1, what happens when the power voltage, V_{DD}, drops below the trip voltage, V_{TRIPF}? Click on your BEST choice.

a) The LVIOUT bit is set to 0
b) The LVIOUT bit is set to 1
c) An interrupt signal is generated
d) A reset signal is generated
e) b and d
f) a and c

Let's complete this tutorial with a question to check your understanding of the material. With the LVI Module enabled and the LVIRSTD bit set to 1, what happens when the power voltage, V_{DD}, drops below the trip voltage, V_{TRIPF}? Click on your best choice.

Answer: The LVI Module sets the LVIOUT bit to 1 when it detects that the power voltage has dropped below the trip voltage. No reset signal is generated since LVIRSTD is set to 1.

Tutorial Completion

- LVI Uses and Features
- LVI Configuration

In this tutorial, you've learned about the features of the LVI Module that help to protect the MCU system during a power voltage drop. You've also learned how to configure the LVI Module using the system configuration register.